SHRI SHANKARACHARYA TECHNICAL CAMPUS, BHILAI

(An Autonomous Institute Affiliated to CSVTU, Bhilai)

SCHEME OF TEACHING AND EXAMINATION (Effective from 2020-2021 Batch)

M.Tech.-Electronics and Telecommunication Engineering (VLSI Design) 4th Semester

S. No.	Boardof Study	Subject	Subject Code	Periods per week			Scheme of Exam			Total Marks	Credit L+(T+P)/2
							Theory/Practical				
				L	T	P	ESE	CT	TA		
1.	Electronics & Telecommunication	Project + Seminar	ET231401	6	-	34	300	-	200	500	23
Total				6		34	300		200	500	23

Note:

(a) Abbreviations used : L-Lecture, T- Tutorial, P- Practical, ESE- End Semester Exam, CT- Class Test, TA- Teacher's Assessment

(b)The duration of end semester examination of all theory papers will be of three hours.

			1.00	Applicable for AY 2021-22 Onwards
Chairman (AC)	Chairman (BoS)	Date of Release	Version	